CIP usage at Cybertrust

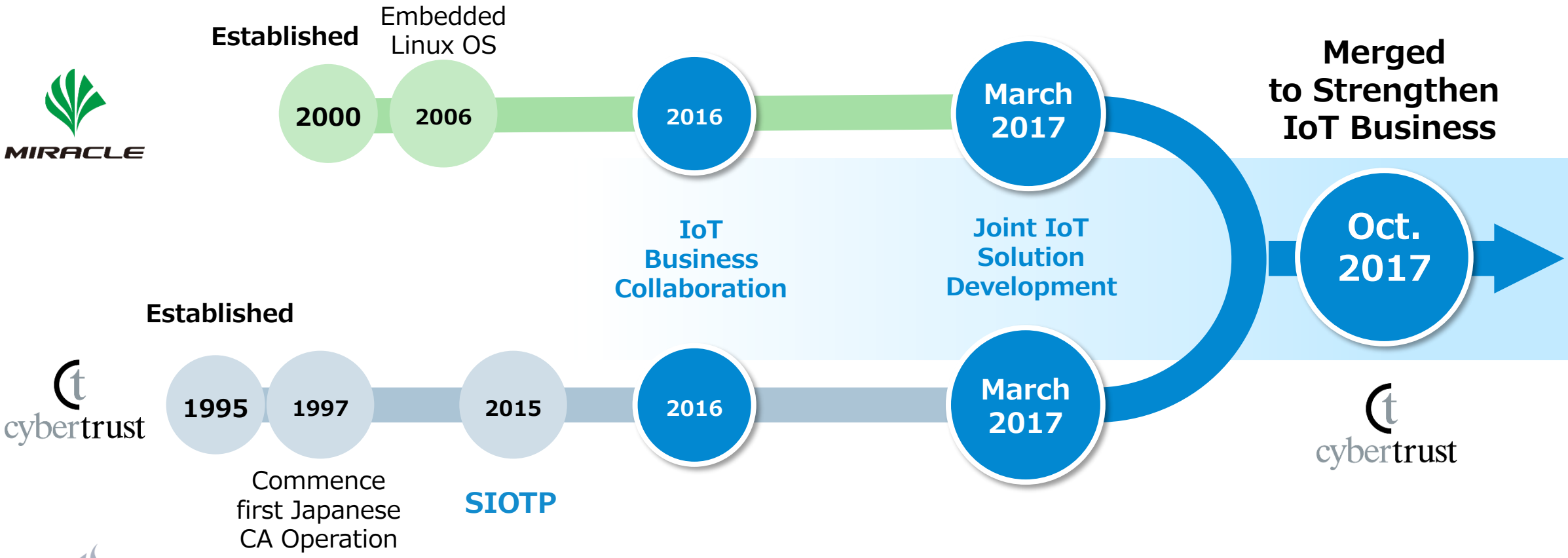
Launching CIP-based Distribution

Masashi Kudo, Cybertrust Japan Co., Ltd.

CIP mini summit 2019, Lyon, 31/10/2019

Who we are ?

Cybertrust is a company who offers the largest Japanese Digital Authentication Infrastructure and Embedded Linux Technology

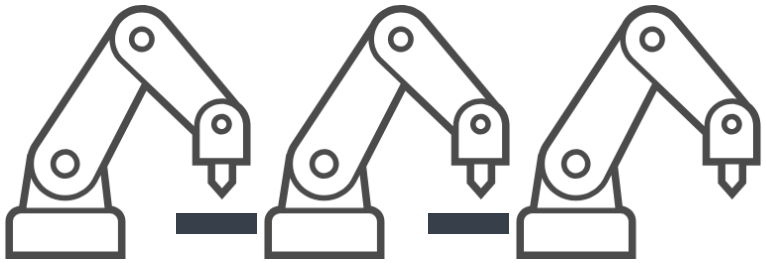


※SIOTP : Secure IoT Platform

CIVIL INFRASTRUCTURE PLATFORM

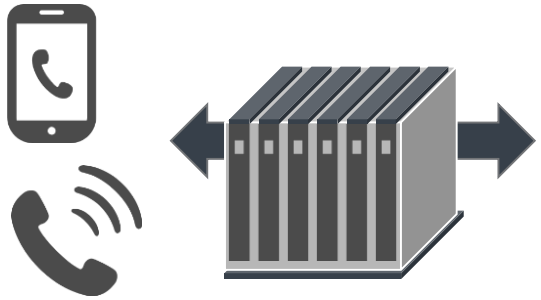
Our customers in embedded areas

Factory Automation



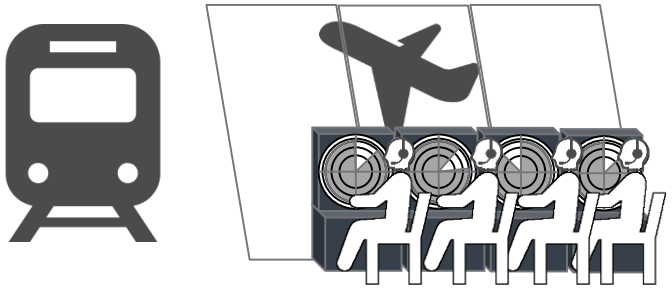
PLC: 15 Years

Communication



PLC: 15 Years

Transportation



PLC: 15 Years

PLC: 20 Years

Automotive

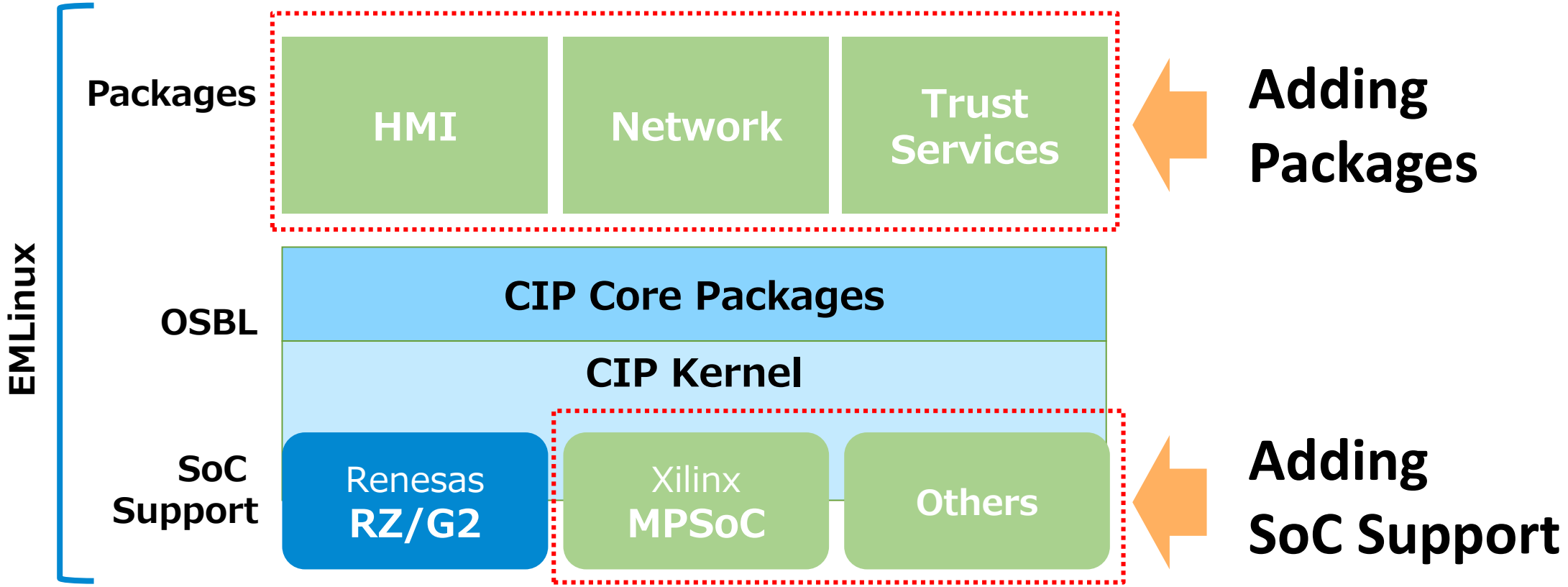
PLC: 20 Years

PLC: Product Life Cycle

EMLinux highlights

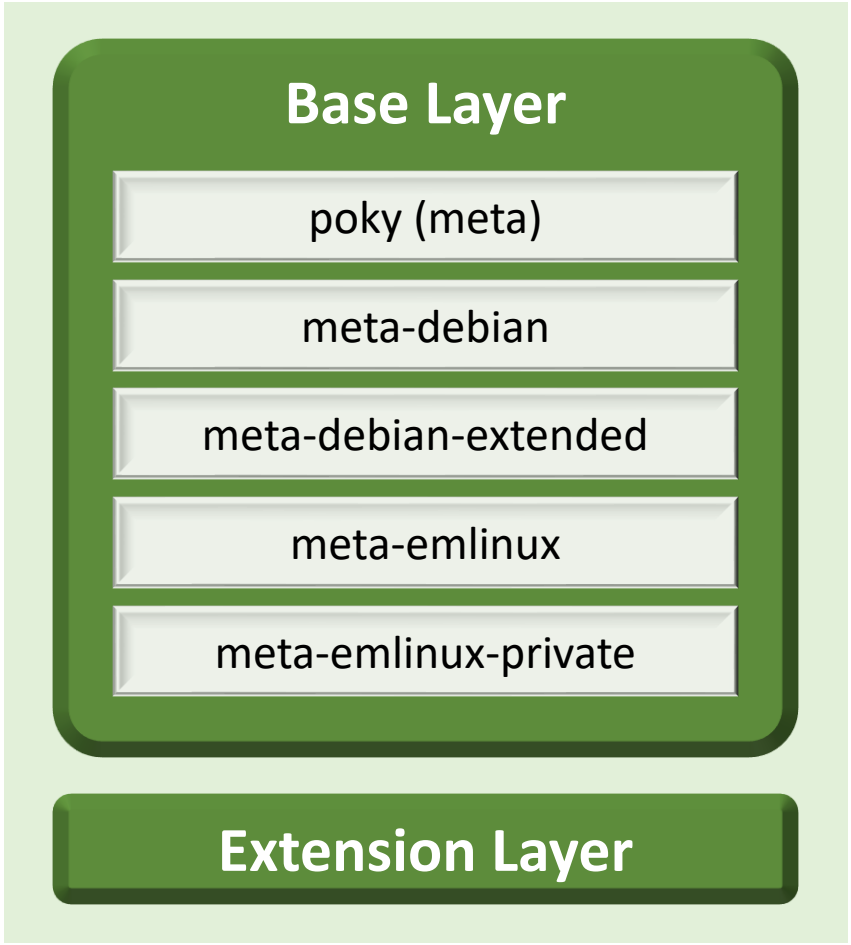
- **EMLinux is CIP-based Linux distribution offered by Cybertrust**
  - Source Distribution: Poky (Yocto) as build system + meta-debian
  - The 1st release was on October 29th
- **Features from CIP**
  - CIP OSBL (CIP SLTS4.19 kernel + CIP core packages)
  - SoC: Renesas RZ/G2
  - IEC 62443-4 Readiness (Coming)
- **Other Features**
  - Additional packages from Debian Buster for HMI and Network
  - Additional SoC support: Xilinx Ultrascale+ MPSoC, qemuarm, qemuarm64, rasberrypi3-64
  - Vulnerability Information Notification & patches for 10 years
  - OTA + Trust Service for Authenticity (Coming)

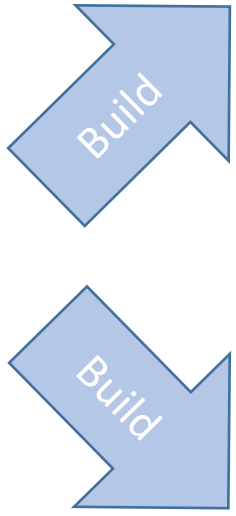
Practices to develop the distribution



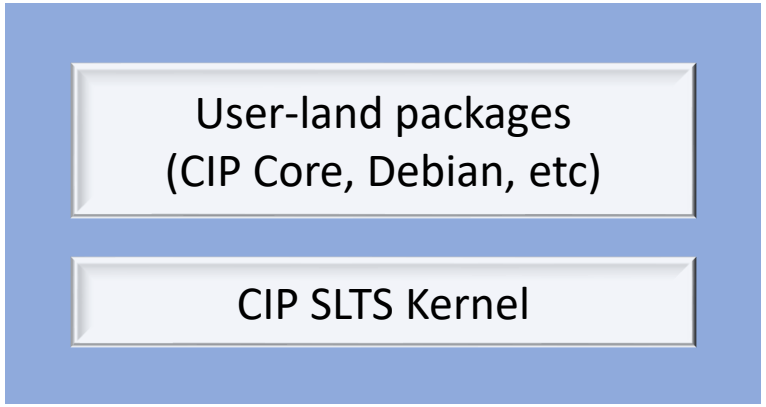
Adding packages

EMLinux Source Distribution



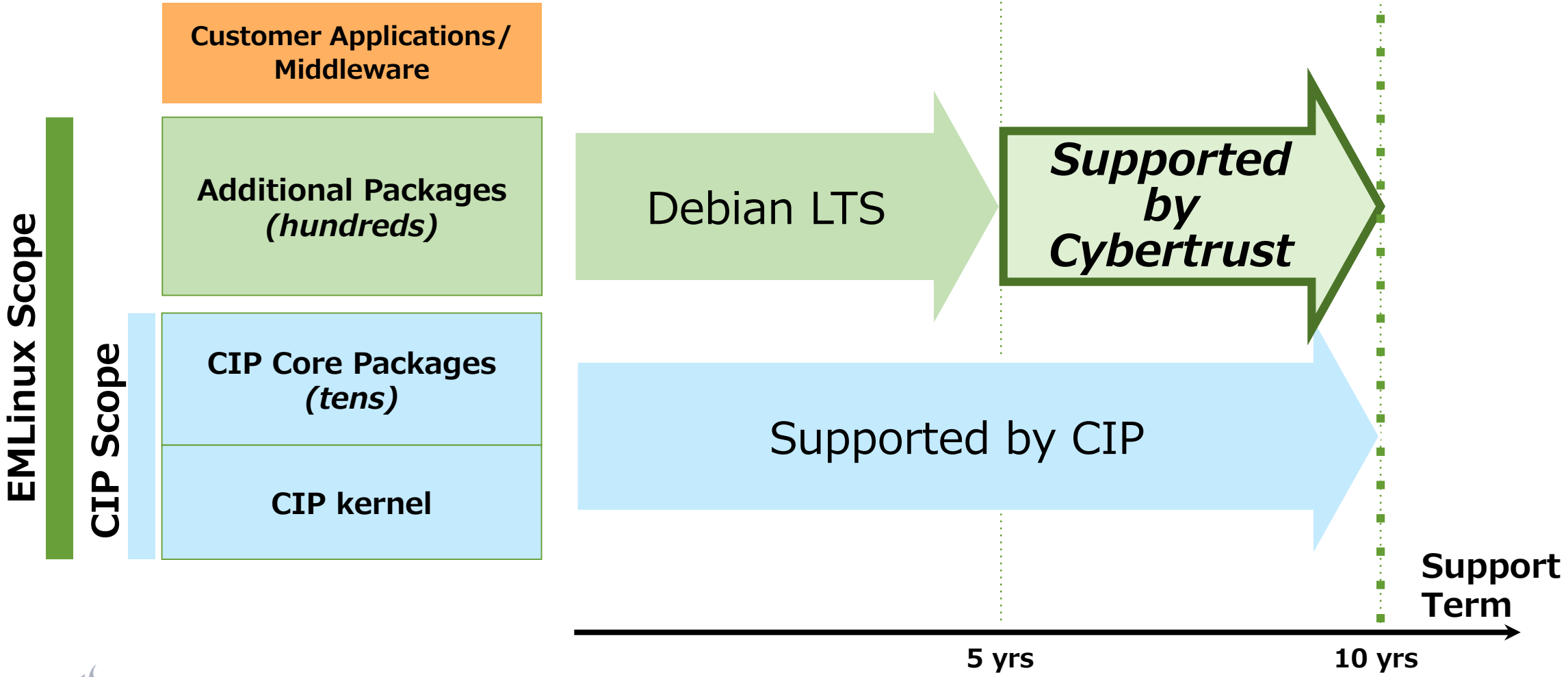


EMLinux Image for Target Device



EMLinux SDK

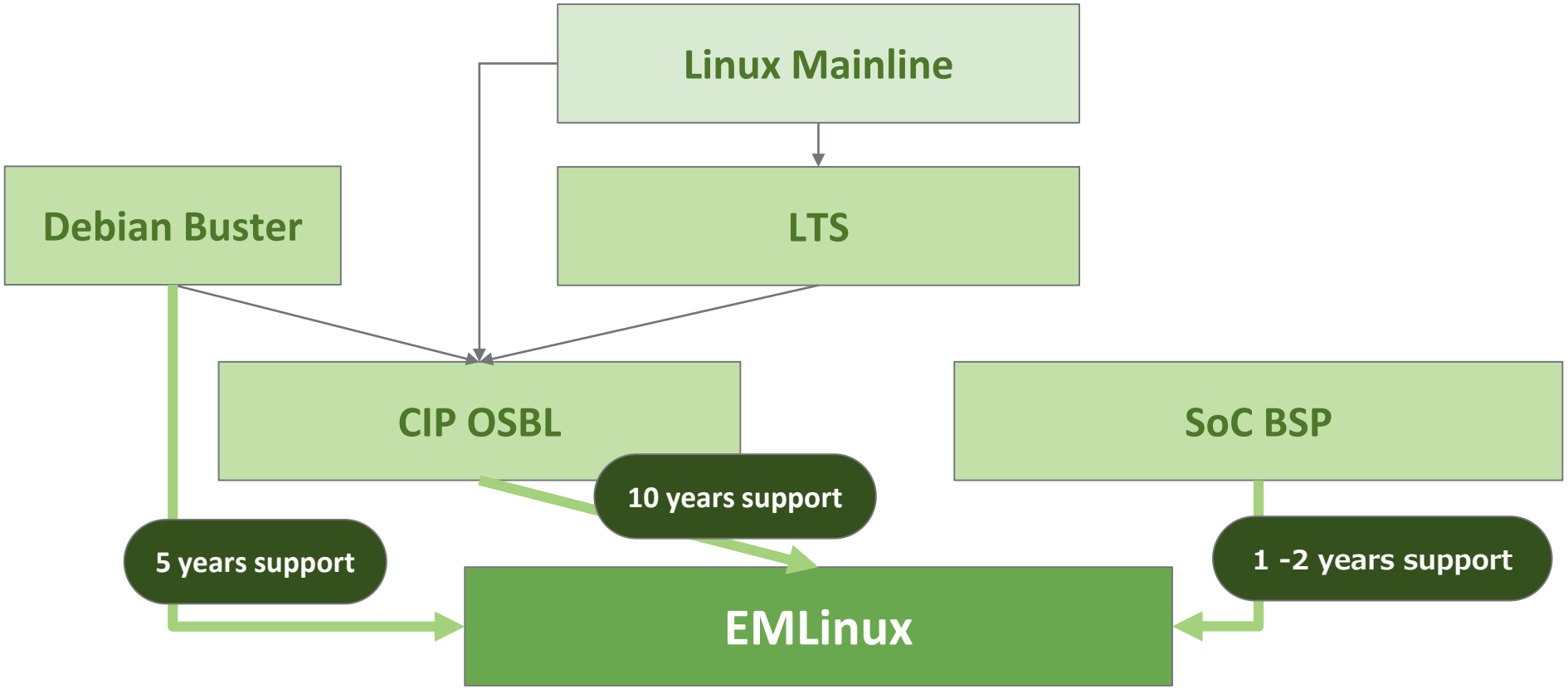
Ten years support



EMLinux supported hardware

CIP Reference Hardware	EMLinux Supprted Hardware
• AM335x Beaglebone Black (Armv7) • QEMU x86_64 • RZ/G1M iWave Qseven Development Kit (Armv7) • RZ/G2M HopeRun HiHope (Armv8) • SIMATIC IPC227E (x86-64) • OpenBlocks IoT VX2 (x86-64)	• **QEMU (ARMv7-A)** • **QEMU (ARMv8-A)** • **Raspberry Pi3 64bit (ARMv8-A)** • **RZ/G2E Silicon Linux ek874 (Armv8)** • RZ/G2M HopeRun HiHope (Armv8) • **Xilinx Zinq Ultrascale+ MPSoC zcu102 (Armv8)**

EMLinux sources



Approach to support non-CIP SoCs

- **Two alternatives to support non-CIP SoCs with EMLinux**
  - **Alt1**) Add SoC board support packages locally
  - **Alt2**) Contribute missing patches to CIP from BSP

- **Would like to take Alt2 for Xilinx Zinq Ultrascale+ MPSoC**
  - Conducted gap analysis between CIP SLTS4.19 and MPSoC BSP kernel
    - Identified missing patches from its BSP for our use cases (HMI and Network)
      - Neary 500 patches required to add to CIP SLTS4.19
  - Proposed the code contribution to the CIP community

Adding SoC support

- The contribution proposal was granted under the following conditions, and we are now preparing for it.

To follow **“Upstream-First”** principle, only patches in Linux Mainline are accepted

Add the target board to CIP test environment for CI

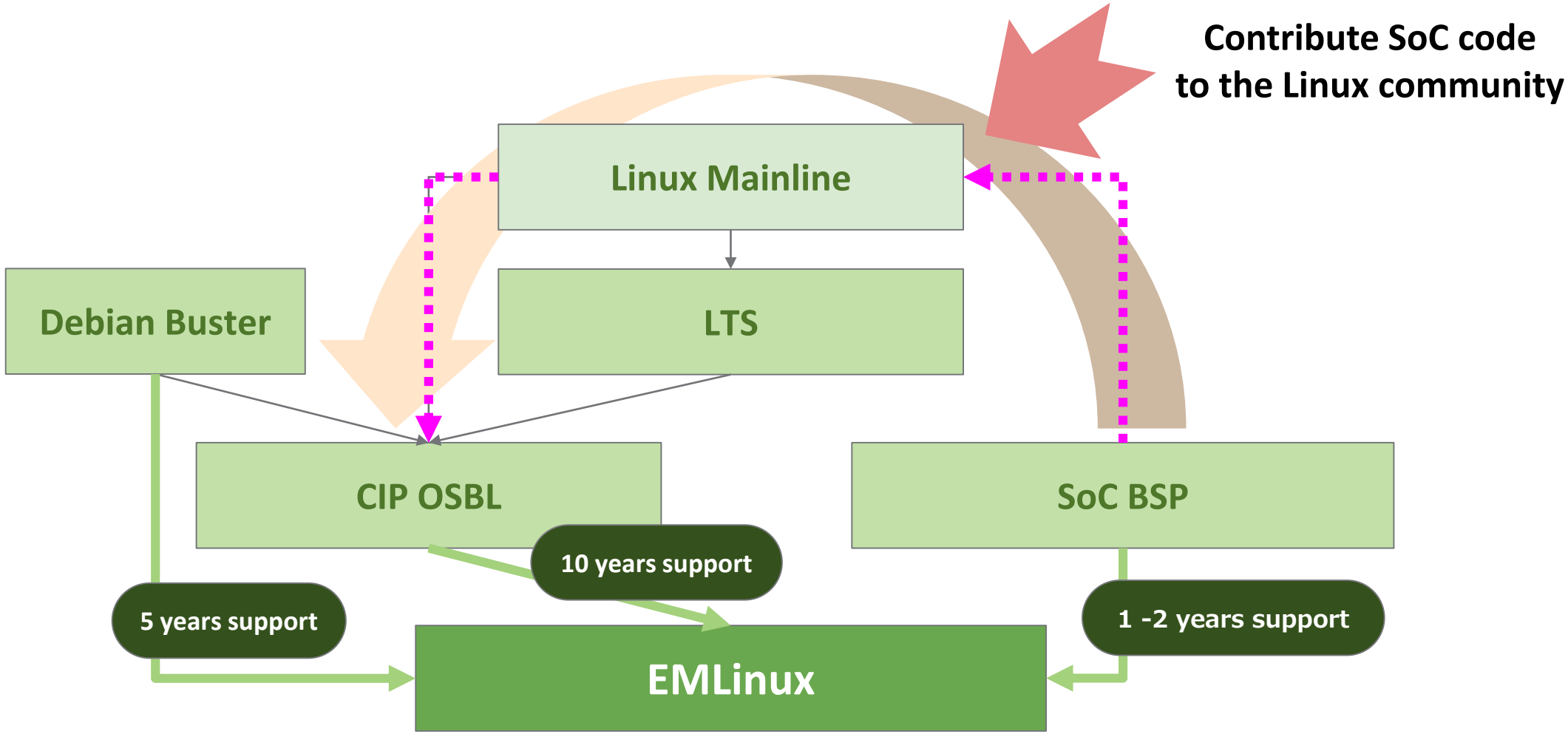
Contribute code of the target board and maintain it

Adding SoC support

- Next Steps (suggested by Pavel-san)

1. Identify minimum usable subset of the patches. That would likely be "whatever is necessary to get some kind of output on serial console", probably clock, pinctrl, serial, dts.
2. Verify that support is already in mainline, submit necessary patches if not.
3. Add this point it may be useful to start running tests of mainline on your LAVA board.
4. Send a list of patches that will be needed for initial boot.
5. Start submitting patches for review & merge.

Adding SoC support from upstreams



What's next

- **In CIP Community:**
  - Proceed to contribute MPSoC code to CIP
    - Consider to contribute code to Linux Mainline where necessary
  - Discuss with SoC vendors for cooperation
  - Refine the guideline to add SoC support in CIP
- **For EMLinux:**
  - Expand target SoCs
    - Investigate an appropriate way to support the SoCs code
  - Add packages for IEC 62443-4 readiness and OTA support

Thanks you!